

09-19-00

A



Patent Application  
Docket No. 34645-00498USPT

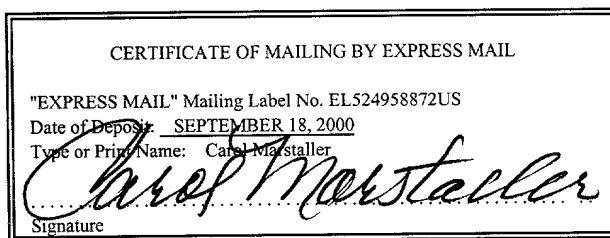
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Jonas Karlsson and Riaz Esmailzadeh

For: **ZERO DELAY INTERFERENCE CANCELLATION**

BOX APPLICATION  
Assistant Commissioner  
for Patents  
Washington, D.C. 20231



Sir:

PATENT APPLICATION TRANSMITTAL LETTER

Transmitted herewith for filing, please find the following:

- X Specification, claims and abstract of the above-referenced patent application (total of 24 pages)
- X 6 sheet(s) of drawing(s) (   formal/ X informal).
- X Combined Declaration and Power of Attorney (unsigned)
- An Assignment of the invention to: \_\_\_\_\_
- \_\_\_\_\_ A verified statement claiming small entity status under 37 CFR 1.9 and 1.27.

\_\_\_\_ Priority is claimed under 35 U.S.C. § 119 based on filing in \_\_\_\_.

	<u>Application No.</u>	<u>Filing Date</u>
(1)		
(2)	____	____
(3)	____	____

\_\_\_\_ (No.) Certified copy (copies) \_\_\_\_ are attached; or \_\_\_\_ were previously filed on \_\_\_\_.

\_\_\_\_ Other (specify): \_\_\_\_

The filing fee has been calculated as shown below:

FOR: <u>LARGE ENTITY</u>	NO. FILED	NO. EXTRA	RATE	FEE
<b>BASIC FEE</b>				<b>\$690</b>
<b>TOTAL CLAIMS</b>	<b>16- 20</b>		<b>\$39</b>	<b>\$</b>
<b>INDEPENDENT CLAIMS</b>	<b>2- 3</b>		<b>\$78</b>	<b>\$</b>
<b>MULTIPLE DEPENDENT CLAIM(S) PRESENTED</b>			<b>\$260</b>	<b>\$ ____</b>
<b>TOTAL FEE:</b>				<b>\$690</b>

\_\_\_\_ Please charge my Deposit Account No. 10-0447 in the amount of \$ \_\_\_\_ This sheet is attached in duplicate.

X A check in the amount of \$690.00 is attached. Please charge any deficiency or credit any overpayment to Deposit Account No. 10-0447.

X The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 10-0447 This sheet is attached in triplicate.

X Any additional filing fees required under 37 CFR 1.16 including fees for presentation of extra claims.

X Any additional patent application processing fees under 37 CFR 1.17 and under 37 CFR 1.20(d).

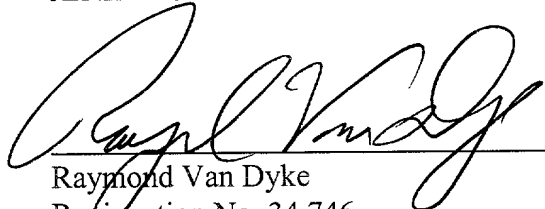
X The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 10-0447. This sheet is attached in duplicate.

X Any patent application processing fees under 37 CFR 1.17 and under 37 CFR 1.20(d).

— The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).

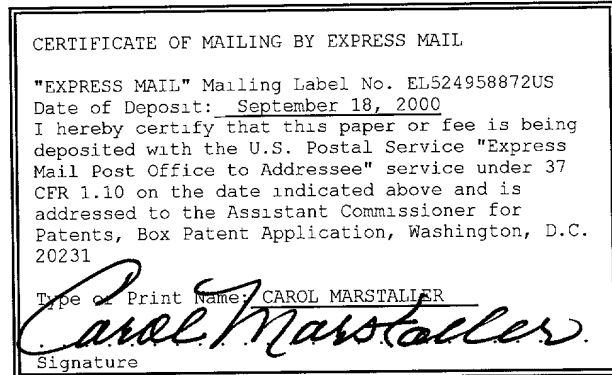
X Any filing fees under 37 CFR 1.16 including fees for presentation of extra claims.

JENKENS & GILCHRIST

  
Raymond Van Dyke  
Registration No. 34,746

Date: September 18, 2000

JENKENS & GILCHRIST  
1445 Ross Avenue, Suite 3200  
Dallas, Texas 75202-2799  
214/855-4708



**ZERO DELAY INTERFERENCE CANCELLATION**

**CROSS-REFERENCES TO RELATED APPLICATIONS**

This Application for Patent claims the benefit of priority from, and hereby incorporates by reference the entire disclosure of, co-pending U.S. Provisional Application  
5 for Patent Serial No. 60/207,703, filed May 26, 2000.

**BACKGROUND OF THE PRESENT INVENTION**

Field of the Invention

The present invention relates to the use of Code  
10 Division Multiple Access (CDMA) techniques in mobile cellular communication systems and, more particularly, to a method and

apparatus for minimizing the delay due to processing of interference cancellation algorithms.

Background of the Invention

Most presently available CDMA cellular communication systems use some type of spread spectrum modulation wherein the encoded information signal is spread over a very wide frequency range during transmission. A unique spreading sequence assigned to each user allows multiple users to transmit simultaneously over the same frequency range. The spread spectrum modulated signals may then be despread using the unique spreading sequences to recover the information signals. The information signals are thereafter decoded back into their original form.

Referring to FIGURE 1, a detector such as a single-user detector 10 or a multiple-user detector 12, can be used to detect the spread spectrum modulated signal and recover the information signal. In general, the single-user detector 10 detects spread spectrum modulated signals on an individual user basis without relying on information about other users. The multiple-user detector 12, on the other hand, detects spread spectrum modulated signals for several users jointly, i.e., information about one user (e.g., bit decisions,

spreading sequences, channel estimates, path profiles, etc.) may also be used for other users.

Referring to FIGURE 2, both the single-user and multiple-user types of detectors generally include a conventional receiver 20, a buffer 22, and a de-interleaver/decoder 24. The conventional receiver 20 receives the spread spectrum modulated signal from an antenna assembly 26 and despreads the signal using standard techniques that are well known to those of ordinary skill in the art. The recovered information signal is then passed to the buffer 22 for temporary storage, and subsequently forwarded to the de-interleaver/decoder 24 for de-interleaving and decoding.

The above method, however, does not take into account information about interfering signals that may be present. For example, if too many users are transmitting simultaneously over the same frequency range, a phenomenon called multiple access interference may begin to degrade system performance. To improve the system performance, special receivers called interference cancellation (IC) receivers may be employed. These IC receivers use special interference cancellation algorithms that make use of information about the spread spectrum modulated signal and

Included among the information used by the interference cancellation algorithms are the spreading sequence mentioned previously and a spreading factor of the spread spectrum modulated signal. The spreading factor, also called the processing gain, is essentially the ratio of the bandwidth of the spread spectrum modulated signal over the bandwidth of the information signal. In general, a higher spreading factor is desirable because the higher the spreading factor, the less susceptible a system will be to interference.

Pallas2 716103 v 2, 34645 00498USPT

may not be acceptable to those services that require short processing delays.

Therefore, it is desirable to be able to minimize any delays incurred in the processing of spread spectrum modulated signals in CDMA cellular systems. More specifically, it is desirable to be able to reduce the processing delay incurred by the interference cancellation algorithms of IC receivers over conventional receivers in such CDMA cellular systems.

**SUMMARY OF THE INVENTION**

The present invention is related to a method and apparatus for minimizing the processing delay incurred by an IC receiver over conventional receivers in a CDMA cellular system. In accordance with the invention, the conventional receiver and the IC receiver are operated in parallel to each other. Data from the conventional receiver are then used to supplement data from the IC receiver in order to minimize the delays incurred by the IC receiver.

In one aspect, the invention is related to a method of reducing signal processing delay time in a CDMA cellular communications system. The method comprises processing a data frame according to a first process, simultaneously



processing the data frame according to a second process, and  
combining selected segments of the data frame processed  
according to the first process with selected segments of the  
data frame simultaneously processed according to the second  
5 process.

In another aspect, the invention is related to a signal  
receiving apparatus for reducing signal processing delay time  
in a CDMA cellular communications system. The apparatus  
comprises a first processor for processing a data frame, a  
10 second processor for simultaneously processing the data  
frame, and a selector coupled to the first and second  
processors, wherein the selector is adapted to combine  
selected segments of the data frame processed by the first  
processor with selected segments of the data frame  
15 simultaneously processed by the second processor.

A more complete appreciation of the present invention  
and the scope thereof can be obtained from the accompanying  
drawings (which are briefly summarized below), the following  
detailed description of the presently-preferred embodiments  
20 of the invention, and the appended claims.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

5       FIGURE 1 illustrates single and multiple user detectors;

FIGURE 2 illustrates a detector having a conventional receiver;

FIGURE 3 illustrates a detector according to one embodiment of the present invention;

10       FIGURE 4 illustrates the timing diagram according to the embodiment of FIGURE 3;

FIGURE 5 illustrates a detector according to another embodiment of the present invention;

15       FIGURE 6 illustrates the timing diagram according to the embodiment of FIGURE 5; and

FIGURE 7 illustrates a flowchart of a selection process according to the embodiment of FIGURE 5.

#### **DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EXEMPLARY EMBODIMENTS**

20       The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This

invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the scope of the invention to those skilled in the art.

As mentioned previously, the present invention provides a way to reduce the processing delay incurred by the IC receiver or, more specifically, by the interference cancellation algorithm of the IC receiver. In accordance with the invention, data from a conventional receiver operating in parallel with the IC receiver may be used to supplement data from the IC receiver. Under this arrangement, delays incurred by the IC receiver in excess of the typical processing time of the conventional receiver may be reduced or entirely eliminated.

Referring now to FIGURE 3, in an exemplary embodiment of the present invention, a detector 30 includes the conventional receiver 20 described above (see FIGURE 2) and an IC receiver 32. The IC receiver 32 employs a special interference cancellation algorithm that uses information about the interfering signals and the spread spectrum modulated signal, including the spreading factor thereof, to

enhance recovery of the information signal. Reception of the spread spectrum modulated signal is effected by the antenna assembly 26 which provides the signal to both the conventional receiver 20 and the IC receiver 32. The  
5 conventional receiver 20 and the IC receiver 32 then process the spread spectrum modulated signal in parallel, and output the recovered information signal to a selector 34.

The selector 34 functions to select between the outputs of the conventional receiver 20 and the IC receiver 32 and  
10 provides the selected output to a buffer 22. In a preferred exemplary embodiment, the selector 34 combines selected portions of the two outputs and provides the combined output to the buffer 22, as will be described further below. The information signal from the selector 34 is then temporarily  
15 stored in the buffer 22 for subsequent de-interleaving and decoding by the de-interleaver/decoder 24. Details of the de-interleaving and decoding processes are well known to those of ordinary skill in the art and will not be described here. Suffice it to say, however, that the de-  
20 interleaver/decoder 24 and the processes performed thereby have been highly optimized such that de-interleaving and decoding of the information signal may be done very quickly and efficiently. Accordingly, one of the functions of the

buffer 22 is to provide a steady queue of information signals that are ready to be processed by the de-interleaver/decoder 24. Therefore, it is expedient that the selector 34 outputs the information signals to the buffer 22 with as little  
5 unnecessary delay as possible.

A better understanding of the operation of the selector 34 may be had with reference to FIGURE 4, wherein a timing diagram illustrates the relative timing of a data frame received and processed by the detector 30. As is well known  
10 to those of ordinary skill in the art, information transmitted over a cellular link may be divided into frames, each frame having a plurality of segments. The frames are received and processed segment by segment on a first in first out basis. In FIGURE 4, the top data frame represents a  
15 received frame 40 having a plurality of segments numbered from 1-10. The second frame represents the received frame 40 after it has been processed by the conventional receiver 20, and will be referred to herein as the conventional frame 42. The third frame also represents the received frame 40,  
20 but after it has been parallel processed by the IC receiver 32, and will be referred to herein as the IC frame 44. Note that the conventional and IC frames 42 and 44 are shifted in time relative to the received frame 40 due to processing

delays, with the IC frame 44 suffering a somewhat larger delay. Finally, the last data frame represents the received frame 40 after it has been provided to the buffer 22, and will be referred to herein as the buffer frame 46.

5 As can be seen, the faster conventional receiver 20 can typically complete processing of the conventional frame 42 at approximately time 'x', whereas the IC receiver 32 does not typically complete processing of the IC frame 44 until approximately time 'y'. Thus, the IC receiver 32 incurs an  
10 incremental delay of time 'd', which is the difference between time 'x' and time 'y', relative to the conventional receiver 20. This incremental delay time 'd' is due, in large part, to the additional processing required by the complex interference cancellation algorithm of the IC  
15 receiver 32. Although some cellular communications systems may be able to efficiently manage the incremental delay, certain commercial systems with strict timing requirements may not be able to handle the extra delay in an efficient manner, if at all. In particular, for systems using  
20 multiple-user type detectors wherein user information is shared among several users, an incremental delay in signal processing for any user may delay or otherwise adversely affect the signal processing for one or several other users.

008160 0029960

In order to avoid such incremental delays, the selector 34 may combine selected segments from both the conventional frame 42 and the IC frame 44. For example, the selector 34 may accept only the first eight segments 1-8 (shaded area) of the IC frame 44 and then obtain the last two segments 9-10 (cross-hatch area) from the conventional frame 42. Because processing of the first eight segments 1-8 of the IC frame 44 will be completed at approximately time 'z', prior to time 'x', no incremental delay will be incurred as a result of the IC receiver 32. In other words, by using a combination of segments, the selector 34 may construct the buffer frame 46 in substantially the same amount time as if only the conventional frame 42 was used. Thus, the present invention is able to provide the enhanced performance associated with the IC receivers while incurring essentially zero delay time relative to conventional receivers.

Although only the first eight segments 1-8 of the IC frame 44 were used in the above example, it should be clear to those of ordinary skill in the art that a different number of segments may be used depending on the complexity of the interference cancellation algorithm and, hence, the delay incurred thereby. Indeed, in the preferred embodiment, the number of segments selected from the IC frame 44 is not a

predefined number; rather the selector 34 may dynamically adjust the number of segments selected as needed to reduce or eliminate the incremental delay time.

In addition to the above incremental delay, a delay may also be incurred due to the requirement that the spreading factor be sent over an entire data frame in the third generation standard for CDMA cellular systems. Recall that the spreading factor, along with other types of information, is used by the interference cancellation algorithm of the IC receiver to despread the spread spectrum modulated signal. Under the third generation standard, the IC receiver would have to wait for an entire data frame to be received to obtain the correct spreading factor and begin despreading that frame. Note that the conventional receiver will also have to wait for the spreading factor, but can thereafter complete the despreading process much faster than the IC receiver.

In order to avoid a delay of an entire data frame, the IC receiver may begin the despreading process based on an estimate of the spreading factor instead of waiting for the correct spreading factor, as will now be described. Referring to FIGURE 5, in another exemplary embodiment of the invention, a detector 50 includes the previously discussed



conventional receiver 20, de-interleaver/decoder 24, antenna  
assembly 26, and IC receiver 32. In addition, the detector  
50 also includes a spreading factor detector 52, a spreading  
factor estimator 54, a first buffer 56a, a second buffer 56b,  
5 and a selector 58, connected as shown. Operation of the  
detection 50 is as follows.

0955300-091800  
The antenna assembly 26 provides a spread spectrum  
modulated signal to the conventional receiver 20 and IC  
receiver 32. The spread spectrum modulated signal is then  
10 despread by the conventional receiver 20 and the IC receiver  
32 in parallel to recover the information signal. As is well  
known to those of ordinary skill in the art, transmission of  
an information signal over a cellular link involves the use  
of a number of channels including a data channel and one or  
15 more control channels. The data channel carries the actual  
data that are to be transmitted, whereas the control channels  
contain administrative information such as the received  
signal strength, synchronization codes, and the correct  
spreading factor. These channels are included in the spread  
20 spectrum modulated signal and are subsequently recovered  
during the despreading process. Data from the data channel  
are then provided to the first buffer 56a, while information

contained in the control channels is passed to the spreading factor detector 52, as shown.

008169-00259660  
0955200-091800

The spreading factor detector 52 functions to extract the correct spreading factor for a frame based on the information contained in the control channels after the entire frame has been received. However, this procedure injects a delay into the despreading process at the IC receiver. Therefore, in accordance with the present invention, instead of waiting for the entire data frame to be received and the correct spreading factor extracted, the IC receiver 32 may begin the despreading process beforehand using an estimate of the spreading factor as provided by the spreading factor estimator 54. The spreading factor estimator 54 estimates the spreading factor using information such as previous spreading factors from earlier data frames, various types of administrative information in the control channel, the power ratio between the control channels and the data channel, detection of the TFCI (transport format combination indicator) bits, and other types of information as represented by the "?" character. A simple initial estimate of the spreading factor for any given data frame may be, for example, the spreading factor of the immediately preceding frame. Then, updated estimates of the spreading

factor may be provided throughout the despreading process as more of the data frame is received. When an estimate of the spreading factor is obtained which is different from that currently being used, the IC receiver 32 will start using the  
5 updated spreading factor instead. The IC receiver 32 then outputs the despread data to the second buffer 56b for temporary storage.

Once a complete frame has been received, the selector  
58 compares the correct spreading factor as extracted by the  
10 spreading factor detector 52 with the estimated spreading factors provided by the spreading factor estimator 54. Preferably the estimated spreading factors and the correct spreading factor will be substantially the same. However, if one or more of the estimated spreading factors are  
15 substantially different from the correct spreading factor, then there is a risk that a large portion or even the entire data frame recovered by the IC receiver 32 may be invalid. In that case, the selector 58 may choose to discard all or a portion of the data frame recovered by the IC receiver 32  
20 as stored in the second buffer 56b and use all or a portion of the data frame recovered by the faster conventional receiver 20 instead, as stored in the first buffer 56a.

Referring now to FIGURE 6, a timing diagram illustrating the relative timing of a data frame received and processed by the detector 50 is shown. The top data frame represents a received frame 60 having a plurality of segments labeled from A-J. The second frame represents the received frame 60  
5 after it has been processed by the conventional receiver 20, and will be referred to herein as the conventional frame 62. The third frame also represents the received frame 60, but after it has been parallel processed by the IC receiver 32, and will be referred to herein as the IC frame 64. Finally,  
10 the last data frame represents the received frame 60 as it is provided to the de-interleaver/decoder 24 by the selector 58, and will be referred to herein as the selected frame 66.

In order to avoid passing an invalid frame or invalid  
15 segments of a frame to the de-interleaver/decoder 24, the selector 58 may combine certain selected segments from both the conventional frame 62 and the IC frame 64. For example, in order to reduce or eliminate any incremental delays, the selector 58 may accept only the first eight segments A-H  
20 (shaded area) of the IC frame 64 and obtain the remaining two segments I-J (cross-hatch area) from the conventional frame 62. In this regard, this portion of the example is similar to the example discussed in connection with FIGURE 4.

However, if the selector 58 determines that the estimated spreading factor used by the IC receiver 32 to despread, say, the first three segments A-C is substantially different from the correct spreading factor, the selector 58 may discard  
5 these three segments and replace them with the first three segments A-C (cross-hatch area) from the conventional frame 62. Accordingly, the selected frame 66 that will be provided to the de-interleaver/decoder 24 will include a number of conventionally despread segments A-C and I-J as well as a  
10 number of segments D-H that have been despread using an interference cancellation algorithm.

FIGURE 7 illustrates the decision-making process of the selector 58. At step 70, an IC frame is obtained. For each segment in the frame, a comparison is made between the  
15 estimated spreading factor used and the actual or correct spreading factor at step 72. If there is a substantial difference between the two spreading factors, the IC frame segment is discarded and the conventional frame segment is selected at step 74. If the two spreading factors are  
20 substantially similar, the IC frame segment is selected at step 76. Once all the frame segments have been selected, the final frame is assembled at step 78. In this way, the present invention is able to provide the enhanced performance

Although the invention has been described with reference  
5 to specific embodiments, various modifications and  
alternatives exist which were not described, but which are  
within the scope and spirit of the invention. Accordingly,  
the invention should be limited only by the following claims.

**WHAT IS CLAIMED IS:**

1           1.    A method of reducing signal processing delay time  
2    in a CDMA cellular communications system, the method  
3    comprising:

4                   processing a data frame according to a first  
5    process;

6                   simultaneously processing said data frame according  
7    to a second process; and

8                   combining selected segments of said data frame  
9    processed according to said first process with selected  
10   segments of said data frame simultaneously processed  
11   according to said second process.

1           2.    The method according to claim 1, further comprising  
2    temporarily storing said combined segments of said data frame  
3    in a buffer.

1           3.    The method according to claim 1, further comprising  
2    de-interleaving and decoding said combined segments of said  
3    data frame.

1           4.    The method according to claim 1, wherein said  
2    combining step includes selecting only segments that were

3 processed not substantially later in time than a completion  
4 of said first process.

1 5. The method according to claim 1, wherein said  
2 second process uses an interference cancellation algorithm.

1 6. The method according to claim 1, further comprising  
2 estimating a spreading factor to be used with said second  
3 process.

1 7. The method according to claim 6, further comprising  
2 detecting a correct spreading factor for said data frame and  
3 comparing said estimated spreading factor with said correct  
4 spreading factor.

1 8. The method according to claim 7, wherein said  
2 segments that were processed using said estimated spreading  
3 factor may be selected only if said estimated spreading  
4 factor is substantially the same as said correct spreading  
5 factor.



1           9. A signal receiving apparatus for reducing signal  
2     processing delay time in a CDMA cellular communications  
3     system, comprising:

4                 a first processor for processing a data frame;

5                 a second processor for simultaneously processing  
6     said data frame; and

7                 a selector coupled to said first and second  
8     processors, said selector adapted to combine selected  
9     segments of said data frame processed by said first processor  
10    with selected segments of said data frame simultaneously  
11    processed by said second processor.

1           10. The apparatus according to claim 9, further  
2     comprising a buffer for temporarily storing said combined  
3     segments of said data frame.

1           11. The apparatus according to claim 9, further  
2     comprising a de-interleaver and a decoder for de-interleaving  
3     and decoding, respectively, said combined segments of said  
4     data frame.

1           12. The apparatus according to claim 9, wherein said  
2     selector is adapted to select only segments that were

3 processed not substantially later in time than a completion  
4 of said first process.

1 13. The apparatus according to claim 9, wherein said  
2 second processor uses an interference cancellation algorithm.

1 14. The apparatus according to claim 9, further  
2 comprising a spreading factor estimator coupled to said  
3 second processor for estimating a spreading factor to be used  
4 by said second processor.

1 15. The apparatus according to claim 14, further  
2 comprising a spreading factor detector for detecting a  
3 correct spreading factor of said data frame, wherein said  
4 selector is further adapted to compare said estimated  
5 spreading factor with said correct spreading factor.

1 16. The apparatus according to claim 15, wherein said  
2 segments that were processed using said estimated spreading  
3 factor may be selected by said selector only if said  
4 estimated spreading factor is substantially the same as said  
5 correct spreading factor.

**ABSTRACT**

Method and apparatus for minimizing the processing delay incurred by an IC receiver over conventional receivers in a CDMA cellular system are disclosed. The method and apparatus  
5 involve operating the conventional receiver and the IC receiver in parallel to each other. Data from the conventional receiver are then used to supplement data from the IC receiver in order to minimize the delays incurred by the IC receiver.

008150 0029950

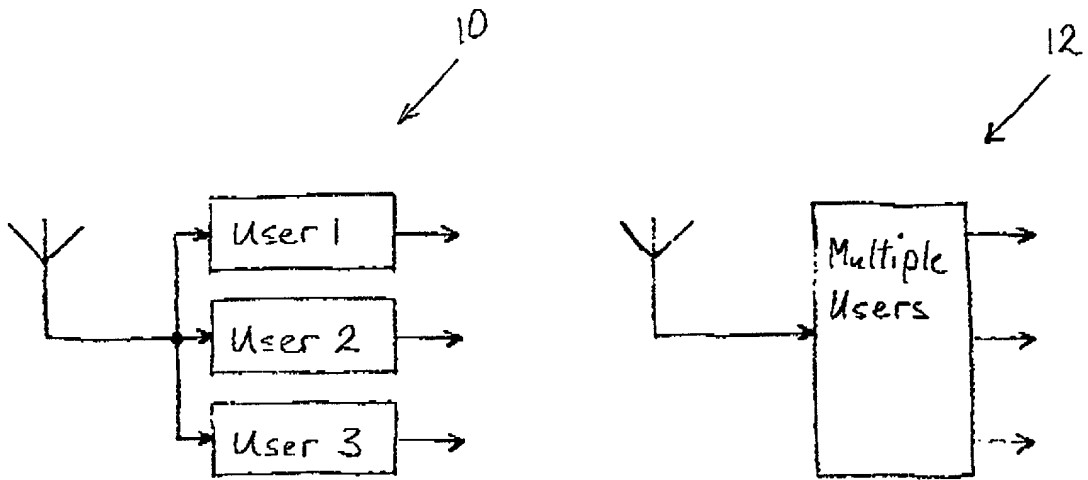


FIG. 1  
(Prior Art)

008760" 00259960

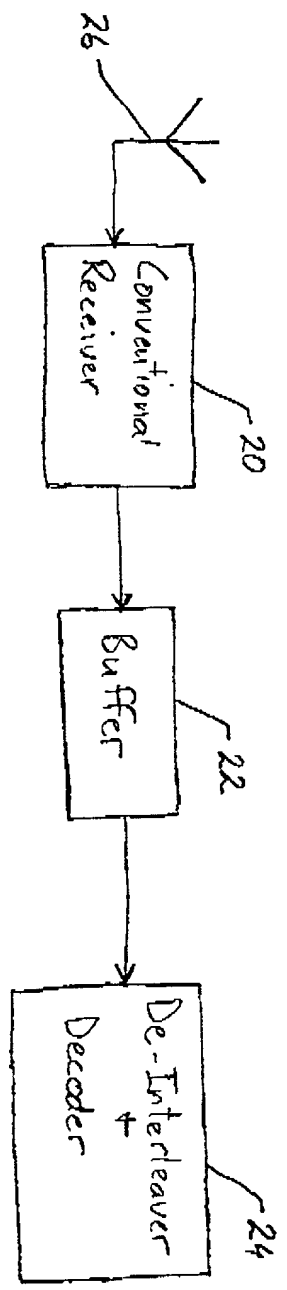


FIG. 2  
(Prior Art)

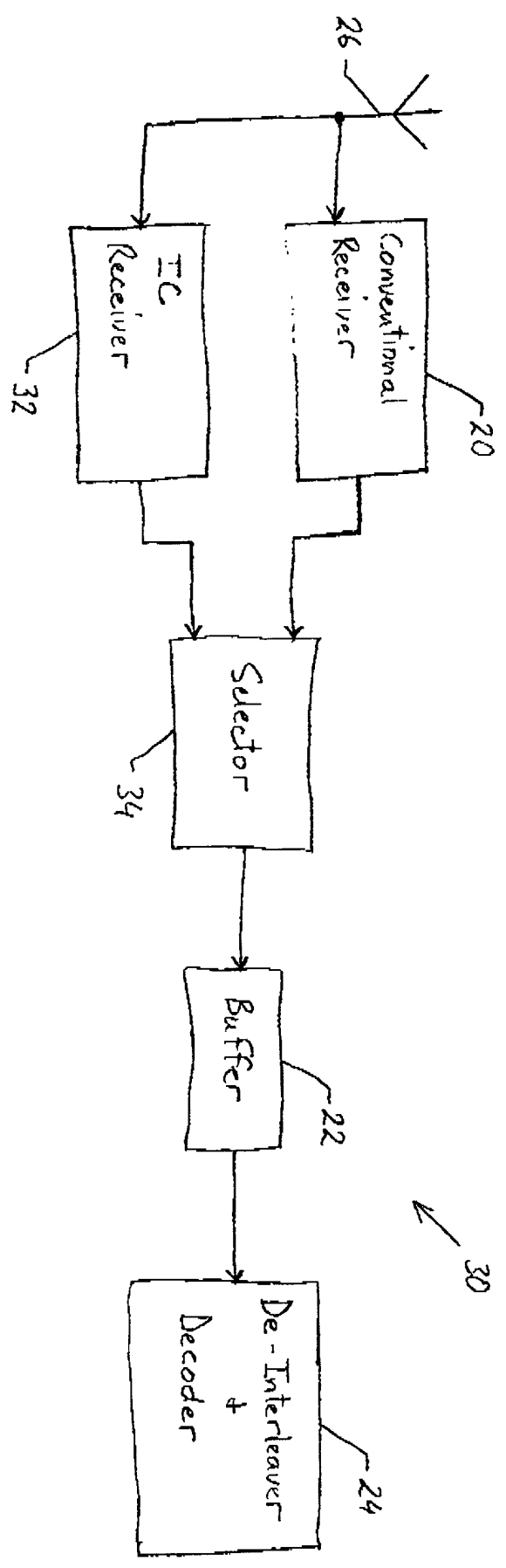


FIG. 3

0965200.091800

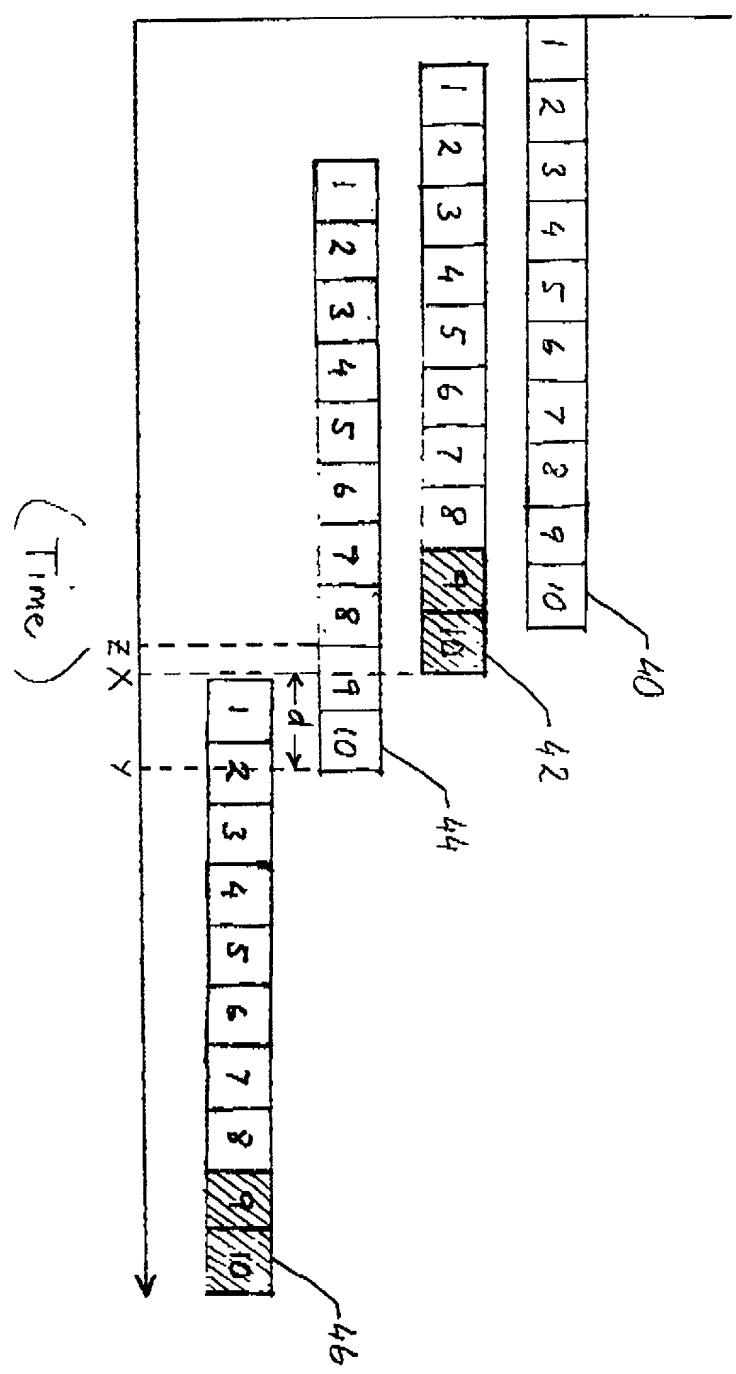


FIG. 4

0965200.091800

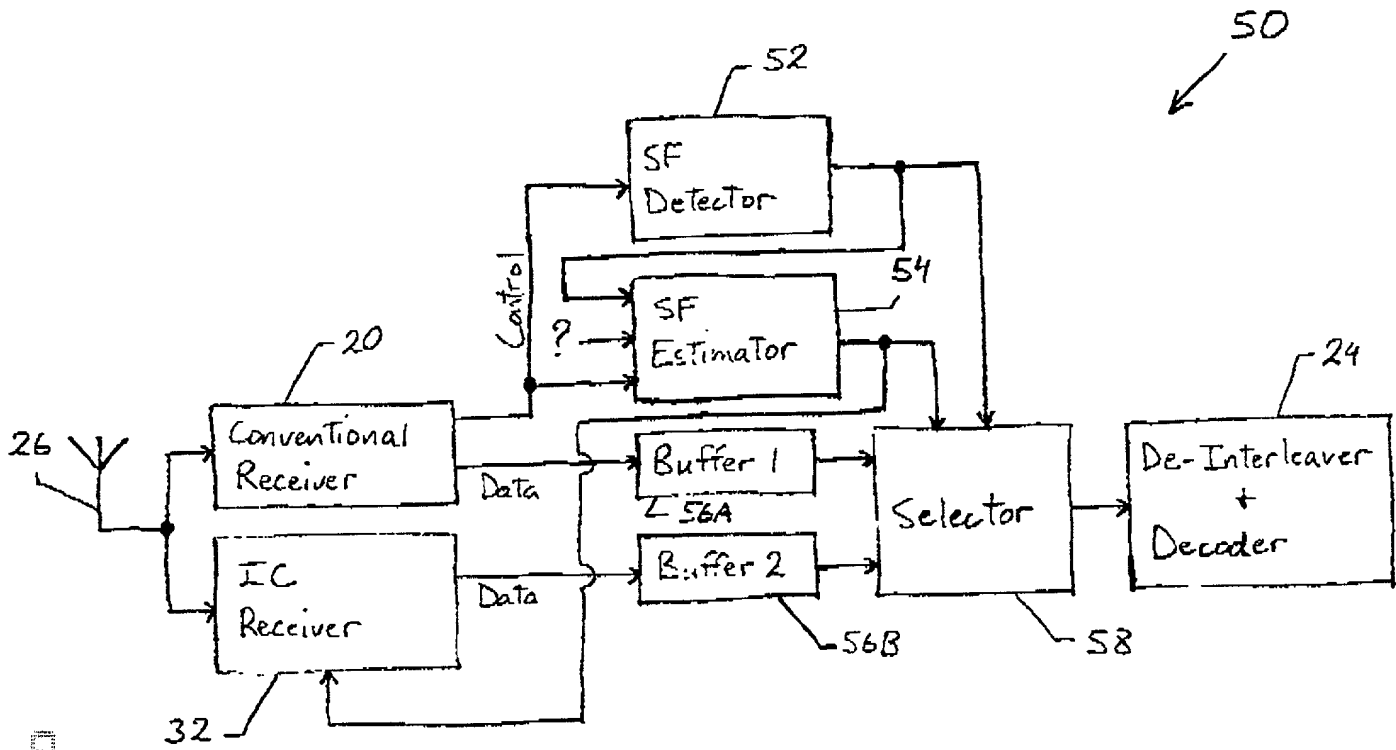


FIG. 5

008160-00259560

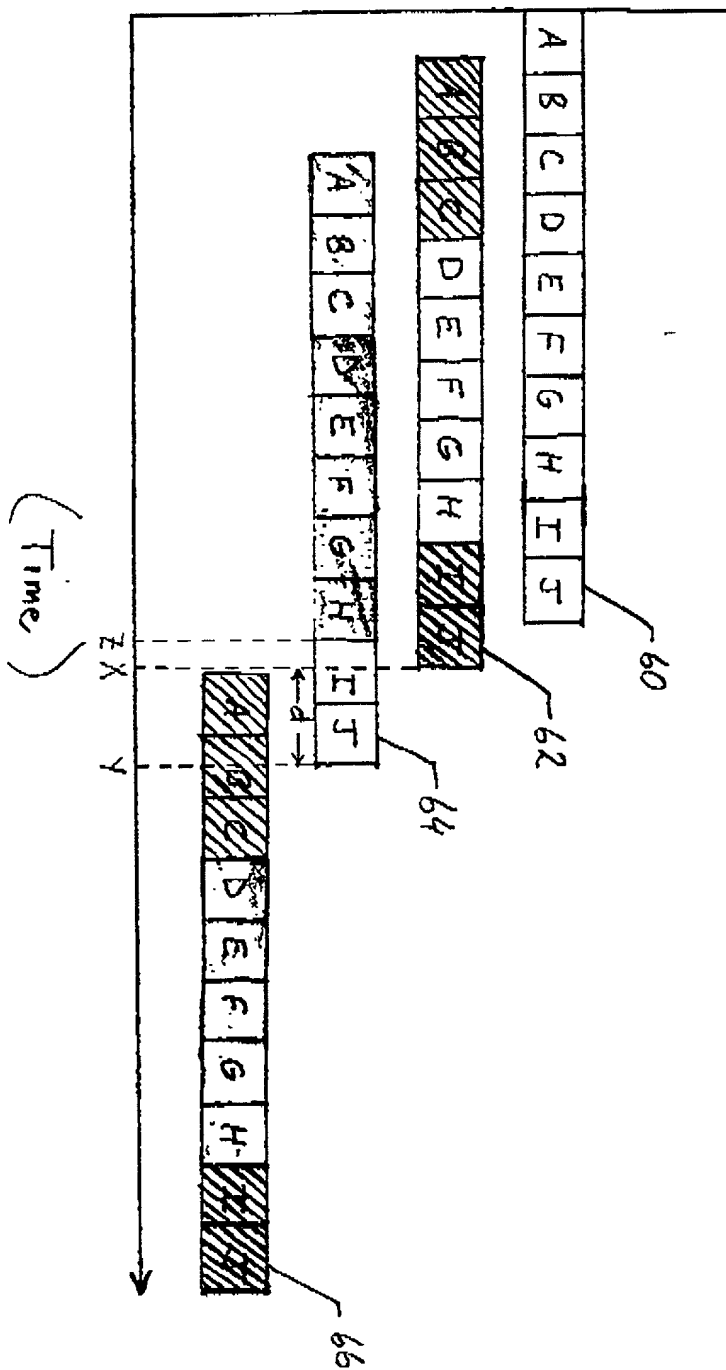


FIG. 6

09565200.091800



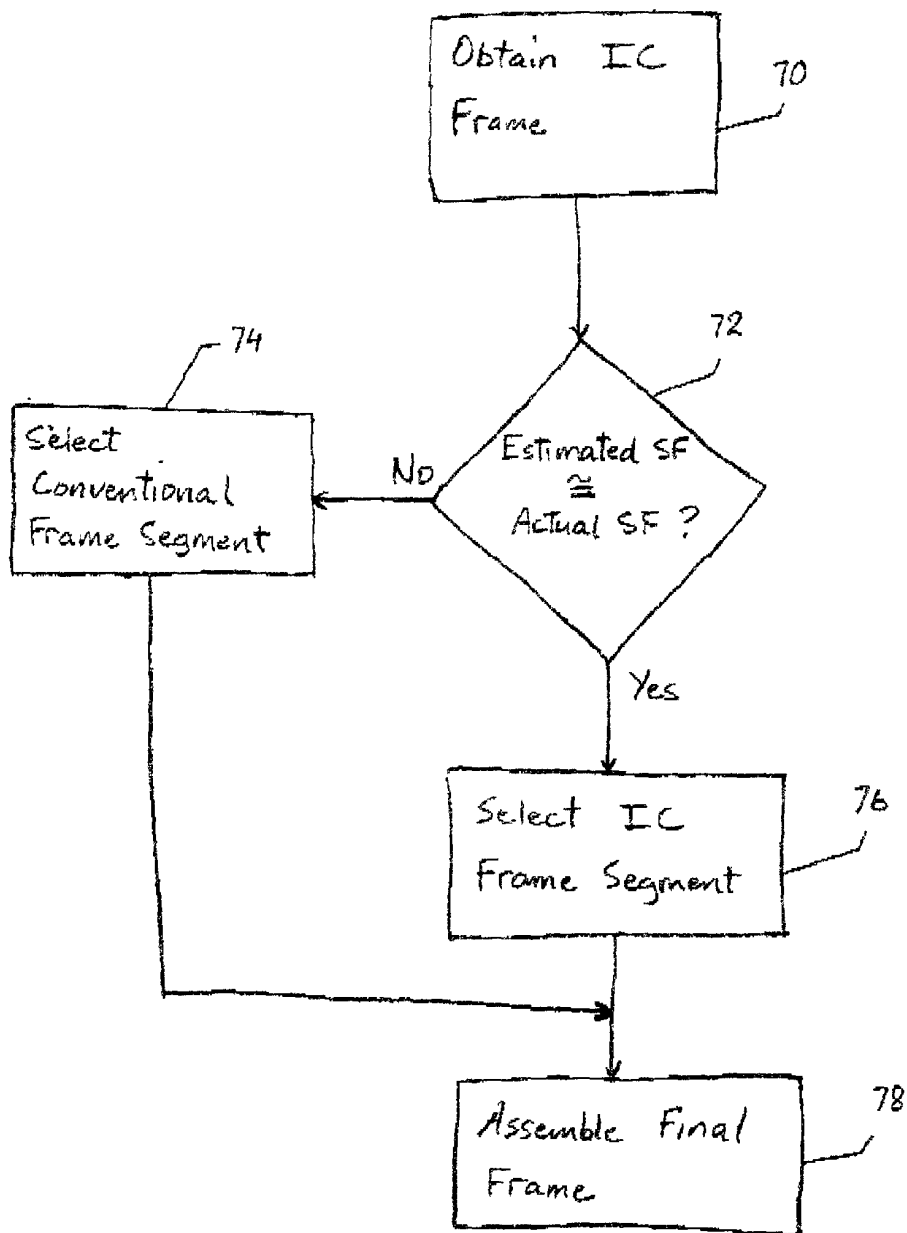


FIG. 7

008150 00259560

**RULES 63 AND 67 (37 C.F.R. 1.63 and 1.67)  
DECLARATION AND POWER OF ATTORNEY**

**FOR UTILITY/DESIGN/CIP/PCT NATIONAL APPLICATIONS**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;  
and

I believe that I am the original, first and sole inventor (if only one name is listed below)  
or an original, first and joint inventor (if plural names are listed below) of the subject matter  
which is claimed and for which a patent is sought on the invention entitled: ZERO DELAY  
INTERFERENCE CANCELLATION, specification of which: (mark only one)

- X   (a) is attached hereto.  
      (b) was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_ and  
was amended on \_\_\_\_\_ (if applicable)  
      (c) was filed as PCT International Application No. PCT/\_\_\_\_\_ on \_  
\_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).  
      (d) was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_  
and was issued a Notice of Allowance on \_\_\_\_\_.  
      (e) was filed on \_\_\_\_\_ and bearing attorney docket number \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above identified  
specification, including the claims as amended by any amendment referred to above or as  
allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the  
patentability of this application as defined in 37 CFR § 1.56. If this is a continuation-in-part  
(CIP) application, insofar as the subject matter of each of the claims of this application is not  
disclosed in the prior United States application in the manner provided by the first paragraph of  
35 U.S.C. § 112, I acknowledge the duty to disclose to the Office all information known to me  
to be material to patentability of the application as defined in 37 CFR § 1.56 which became  
available between the filing date of the prior application and the national or PCT international  
filing date of this CIP application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119/365 of any foreign  
application(s) for patent or inventor's certificate listed below and have also identified below  
any foreign application for patent or inventor's certificate filed by me or my assignee  
disclosing the subject matter claimed in this application and having a filing date (1) before that

of the application on which my priority is claimed or, (2) if no priority is claimed, before the filing date of this application:

PRIOR FOREIGN PATENTS

<u>Number</u>	<u>Country</u>	<u>Month/Day/Year Filed</u>	<u>Date first laid-open or Published</u>	<u>Date patented or Granted</u>	<u>Priority Claimed</u>	
					<u>Yes</u>	<u>No</u>
_____	_____	_____	_____	_____	_____	_____

I hereby claim the benefit under 35 U.S.C. § 120/365 of any United States application(s) listed below and PCT international applications listed above or below:

PRIOR U.S. OR PCT APPLICATIONS

<u>Application No. (series code/serial no.)</u>	<u>Month/Day/Year Filed</u>	<u>Status(pending, abandoned, patented)</u>
60/207,703	May 26, 2000	Pending

I hereby appoint:

TIMOTHY G. ACKERMANN, Reg. No. 44,493  
THOMAS E. ANDERSON, Reg. No. 37,063  
BENJAMIN J. BAI, Reg. No. 43,481  
MICHAEL J. BLANKSTEIN, Reg. No. 37,097  
MARY JO BOLDINGH, Reg. No. 34,713  
MARGARET A. BOULWARE, Reg. No. 28,708  
ARTHUR J. BRADY, Reg. No. 42,356  
MATTHEW O. BRADY, Reg. No. 44,554  
DANIEL J. BURNHAM, Reg. No. 39,618  
THOMAS L. CANTRELL, Reg. No. 20,849  
RONALD B. COOLLEY, Reg. No. 27,187  
THOMAS L. CRISMAN, Reg. No. 24,846  
STUART D. DWORK, Reg. No. 31,103  
WILLIAM F. ESSER, Reg. No. 38,053  
ROGER J. FRENCH, Reg. No. 27,786  
JANET M. GARETTO, Reg. No. 42,568  
JOHN C. GATZ, Reg. No. 41,774  
RUSSELL J. GENET, Reg. No. 42,571

GERALD H. GLANZMAN, Reg. No. 25,035  
J. KEVIN GRAY, Reg. No. 37,141  
STEVEN R. GREENFIELD, Reg. No. 38,166  
JOSHUA A. GRISWOLD, Reg. No. 46,310  
J. PAT HEPTIG, Reg. No. 40,643  
SHARON A. ISRAEL, Reg. No. 41,867  
JOHN R. KIRK JR., Reg. No. 24,477  
PAUL R. KITCH, Reg. No. 38,206  
TIMOTHY M. KOWALSKI, Reg. No. 44,192  
JAMES F. LEA III, Reg. No. 41,143  
HSIN-WEI LUANG, Reg. No. 44,213  
ROBERT W. MASON, Reg. No. 42,848  
ROGER L. MAXWELL, Reg. No. 31,855  
ROBERT A. McFALL, Reg. No. 28,968  
STEVEN T. McDONALD, Reg. No. 45,999  
LISA H. MEYERHOFF, Reg. No. 36,869  
STANLEY R. MOORE, Reg. No. 26,958  
RICHARD J. MOURA, Reg. No. 34,883  
MARK V. MULLER, Reg. No. 37,509  
P. WESTON MUSSELMAN JR. Reg. No. 31,644

DANIEL G. NGUYEN, Reg. No. 42,933  
SPENCER C. PATTERSON, Reg. No. 43,849  
RUSSELL N. RIPPAMONTI, Reg. No. 39,521  
ROSS T. ROBINSON, Reg. No. 47,031  
STEPHEN G. RUDISILL, Reg. No. 20,087  
HOLLY L. RUDNICK, Reg. No. 43,065  
J.L. JENNIE SALAZAR, Reg. No. 45,065  
KEITH W. SAUNDERS, Reg. No. 41,462  
JERRY R. SELINGER, Reg. No. 26,582  
GARY B. SOLOMON, Reg. No. 44,347  
STEVE Z. SZCZEPANSKI, Reg. No. 27,957  
ANDRE M. SZUWALSKI, Reg. No. 35,701  
ALAN R. THIELE, Reg. No. 30,694  
TAMSEN VALOIR, Reg. No. 41,417  
RAYMOND VAN DYKE, Reg. No. 34,746  
BRIAN D. WALKER, Reg. No. 37,751  
GERALD T. WELCH, Reg. No. 30,332  
HAROLD N. WELLS, Reg. No. 26,044  
WILLIAM D. WIESE, Reg. No. 45,217

all of the firm of **JENKENS & GILCHRIST, P.C.**, 3200 Fountain Place, 1445 Ross Avenue, Dallas, Texas 75202-2799, as my attorneys and/or agents, with full power of substitution and revocation, to prosecute this application, provisionals thereof, continuations, continuations-in-part, divisionals, appeals, reissues, substitutions, and extensions thereof and to transact all business in the United States Patent and Trademark Office connected therewith, to appoint any individuals under an associate power of attorney and to file and prosecute any international patent application filed thereon before any international authorities, and I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sent this case to them and by

whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary.

Please address all correspondence and direct all telephone calls to:

Raymond Van Dyke  
Jenkins & Gilchrist, P.C.  
3200 Fountain Place  
1445 Ross Avenue  
Dallas, Texas 75202-2799  
214/855-4708 214/855-4300 (fax)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**NAMED INVENTOR(S)**

1	Jonas Karlsson		
	<b>Full Name</b>	<b>Inventor's Signature</b>	<b>Date</b>
	Marine City B-1305, Shiba-cho, Kanazawa-ku 236-0012 Yokohama Japan <b>Residence</b> (city, state, country)		
2	Riaz Esmailzadeh		
	<b>Full Name</b>	<b>Inventor's Signature</b>	<b>Date</b>
	1-1-25-111 Ooka, Minami-ku 232-0061 Yokohama Japan <b>Residence</b> (city, state, country)		
Marine City B-1305, Shiba-cho, Kanazawa-ku 236-0012 Yokohama Japan <b>Post Office Address</b> (include zip code)			
1-1-25-111 Ooka, Minami-ku 232-0061 Yokohama Japan <b>Post Office Address</b> (include zip code)			